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High Performance DDR3 SDRAM Controller from Eureka Technology Supports AHB and AXI Bus Interface

Eureka Technology Inc., a leading provider of system connectivity intellectual property (IP) cores, today announced its latest DDR3 SDRAM controller core for high performance ASIC/SoC applications.

DDR3 is the latest SDRAM technology with significantly higher data bandwidth and improved power saving over the previous SDRAM generations. Eureka's DDR3 SDRAM controller is designed specifically to harness the performance advantage of the DDR3 SDRAM. It employs high speed design techniques such as fast page access, pipeline design and smart arbitration. The controller supports both DDR2 and DDR3 SDRAMs to enable a smooth transition between the two SDRAM technologies. The highly programmable IP core preserves our customer's investment in the new DDR3 technology as the SDRAM technology continues to evolve.

"Eureka Technology has provided SDRAM controller solutions to customers for over 10 years", said Simon Lau, President of Eureka Technology. "The latest DDR3 SDRAM controller is built upon this tradition of high performance and highly customizable memory subsystem design. The many optional features available in this IP core differentiate itself by providing different configurations of the IP core to meet each and every customer’s application requirements."

The DDR3 controller is licensed in Verilog or VHDL RTL code format. It is synthesizable to virtually any ASIC and FPGA technology and supports the standard DFI PHY interface for easy system integration. Customers of this IP core can choose among many optional features to configure the IP core to their exact specification. Optional features include different user interfaces such as AXI, AHB and generic user interface. The core is available as a single port SDRAM controller or a multi-port SDRAM controller with different bus interfaces at different bus clock speed sharing the same memory.