eNewsletter

KAL - Large IP Cores:

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**

IP Review – CAN FD

The DCAN FD by Digital Core Design (dcd.pl) is a standalone controller for the Controller Area Network (CAN), widely used in automotive and industrial applications. It conforms to Bosch CAN 2.0B specification (2.0B Active) and CAN FD (flexible data-rate). The improved proto-col overcomes standard CAN limits: data can be transmitted faster than with 1 Mbit/s and the pay-load (data field) is up to 64 byte long and limited to 8 byte anymore. When only one node is transmit-ting, the bit-rate can be increased, because no nodes need to be synchronized. Of course, before the transmission of the ACK slot bit, the nodes need to be re-synchronized. The core has a simple CPU interface (8/16/32 bit configurable data width), with small or big endian addressing scheme. Hardware message filtering and 128 byte receive FIFO enable back-to-back message recep-tion, with minimum CPU load. The DCAN FD is described at RTL level, allowing target use in FPGA or ASIC technologies.

FEATURES

- Designed in accordance to ISO 11898-1:2015
- Supports CAN 2.0B and CAN FD frames
- Support up to 64 bytes data frames
- Flexible data rates supported
- 8/16/32-bit CPU slave interface with small or big endianness
- Simple interface allows easy connection to CPU
- Supports both standard (11-bit identifier) and extended (29 bit identifier) frames
- Data rate up to 8 Mbps
- Hardware message filtering (dual/single filter)
- 128 byte receive FIFO and transmit buffer
- Overload frame is generated on FIFO overflow
- Normal & Listen Only Mode
- Transceiver Delay Compensation up to three data bit long
- Single Shot transmission
- Ability to abort transmission
- Readable error counters
- Last Error Code
- Fully synthesizable
- Static synchronous design with positive edge clock-ing and synchronous reset
- No internal tri-states
- Scan test ready

- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Modulation:

- **ADPSM**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

Contact us for data sheet

More information:

http://dcd.pl/ipcore/131/dcan-fd/

KAL is representing DCD.

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Until the next eNews,

Thanks you for your attention.

KAL