eNewsletter

KAL - Large IP Cores:

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C Master/Slave**

IP Review – LCD 32 Controller

The DCD's DBLCD32 core is a fully configurable, uni-versal LCD/TFT display controller. It supports a wide range of resolution and enables both, horizontal and vertical synchronization parameters setup. The dis-play's pixel clock can be generated by an internal pixel clock divider based on the bus clock, or deliv-ered to the core by a dedicated pin. Additionally there is a possibility of using an externally generated pixel clock. Polarization of the generated pixel clock, as well as synchronization signals, is configurable. The DBLCD32 has a DMA capable master interface, which can be used to access a framebuffer placed directly in a system memory. Embedded DMA con-troller has configurable FIFO to store pixels data, which increases system throughput and perfor-mance. Transmission on the master interface is burst oriented and there is a possibility of defining the burst size limit. Data fetched by the DMA inter-face can be translated to 24-bits RGB signals, de-pending on the selected color mode. There are three standard color modes supported: 24-bits True Color, 16-bits(5-6-5) High Color and 8-bits index color mode. Additionally, a 32-bit True Color is also sup-ported, but the MSB byte of each four byte word is ignored. In case of the Indexed Color Mode the DBLCD32 is equipped with pixel palette RAM which is used to translate each byte from the display buffer into 24-bit RGB output. There are two differ-ent formats of color palettes available. The core supports the page flipping mechanism, which ena-bles the usage of multiple buffering totally without the tearing effect. There is also a set of programma-ble interrupts available related to both display syn-chronization and DMA status signals. The core is capable to work on both little and big endian sys-tems. To increase the system performance and flexi-

- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Modulation:

- **ADPSM**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

Contact us for data sheet

bility of usage, the DLBLCD32 can be configured in two possible optimization levels, to find a proper balance between a gate count and a critical path length.

FEATURES

♦ 24-bit RGB interface
♦ Configurable display resolution
♦ Configurable horizontal sync length and blanking
♦ Configurable vertical sync length and blanking
♦ Configurable RGB signals polarization
♦ Configurable pixel clock polarization
♦ Internal pixel clock divider
♦ Different pixel clock modes
♦ DMA capable interface
♦ Configurable DMA FIFO
♦ Configurable burst size limit
♦ AHB bus interface(32-bit)
♦ 24-bit True Color mode support
♦ 16-bit (5-6-5) High Color mode support
♦ 8-bit Indexed Color mode support
♦ 32-bit True Color mode support (one byte ignored)
♦ Pixel palette RAM
♦ Page flipping support
♦ Programmable interrupts
♦ Big and little-endian support
♦ Two different optimization levels
♦ Fully synthesizable, synchronous design

More information:

http://dcd.pl/ipcore/133/dblcd32/

KAL is representing DCD.

www.dcd.pl

www.KALtech.co.il

We are looking forward to hear from you.
Contact us for more information.

Tel +972-77-7199944

http://www.KALtech.co.il

info@kaltech.co.il

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Until the next eNews,

Thanks you for your attention.

KAL