A Reliable ASIC Partner KAL Kataev Associates 15 YEARS

eNewsletter

KAL - Large IP Cores:

VIP cores:

- PCIe, USB, AMBA
- SD/SDIO, eMMC
- UniPro, I3C, Soundwire
- DDR 2/3/4, LPDDR, ONFI, SATA
- HDMI
- CAN, CANFDm FLexRay
- SPI, I2C, SMbus

Memory Controllers:

- **SD/SDIO Controller**
- **SDRAM Controller**
- **DDR / SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

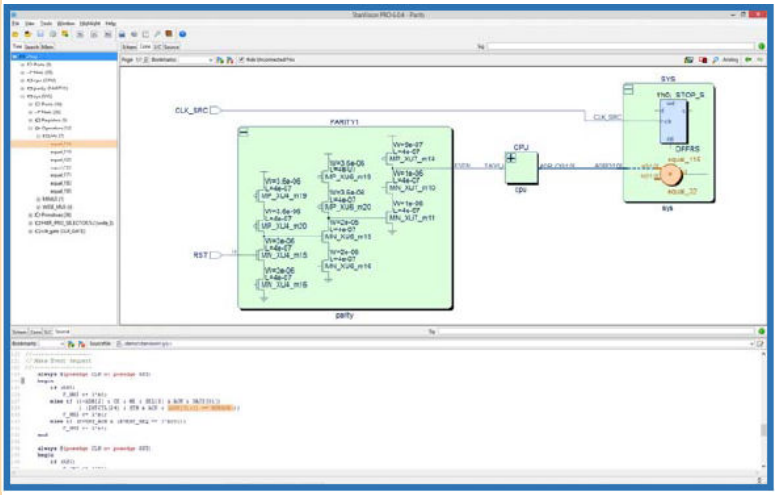
CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588Master/Salve**

StarVision® PRO: A Customizable Mixed-Signal Debugging Platform



StarVision PRO provides engineers with the ability to quickly and easily understand and debug mixed-mode designs and to integrate IP building blocks into their complex SoCs and ICs.

All-in-One - Due to the increasing use of building blocks in SoC design, engineers need to work at different design levels (RTL, gate, transistor, analog, parasitic) as well as with different design languages and netlist formats. To support this challenge, Concept Engineering developed StarVision PRO, an integrated debugging cockpit for mixed-signal and digital design that makes analysis and debugging of complex SoC and IC designs easy and more transparent.

Easy Design Exploration – The interactive design navigation window shows schematic fragments of just the critical portion of the design while, at the same time, providing links to the original source code fragments (RTL, Netlist, SPICE) and to simulation results.

- Verilog-AMS, SystemVerilog, VHDL, SPICE, HSPICE®, ELDO, Spectre®
- AMS viewer, RTL viewer, Netlist viewer and SPICE viewer in one tool
- Mixed-Signal Debugger – Makes IP-based design more transparent
- 64-bit database handles today's largest SoCs and ASICs
- Integrated Waveform Viewer with source code link and

- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Modulation:

- **ADPSM**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are**

schematic link
- Customizable netlist pruning (Verilog, SPICE, SPEF, DSPF)
- Advanced batch processing for automated tool flow
- Tcl based API for user-defined electrical rule checks and customization

KAL is representing Concept Engineering GmbH in Israel.

www.KALtech.co.il

We are looking forward to hear from you.
Contact us for more information.

Tel +972-77-7199944 / 054-6305787 (Adi)

http://www.KALtech.co.il
akatav@kaltech.co.il

Follow on LinkedIn

eNews Registration: **http://www.kaltech.co.il/**

Until the next eNews,

Thanks you for your attention.

KAL

available – Please contact us.

- **We are expert in custom analog IP**

Contact us for data sheet