eNewsletter

KAL - Large IP Cores:

VIP cores:

- **PCIe, USB, AMBA**
- **SD/SDIO, eMMC**
- **UniPro, I3C, Soundwire**
- **DDR 2/3/4, LPDDR, ONFI, SATA**
- **HDMI**
- **CAN, CANFDm FLexRay**
- **SPI, I2C, SMbus**

Military/Aerospace

- **1553**

Multimedia

- **H.264**
- **JPEG**

Automotive:

- **CAN/CAN-FD**
- **FlexCAN**
- **FlexRay**
- **Lin**

AHB/APB Peripherals:

- **AHB/AXI/APB bridges**
- **Inter Connect complete IP**

Memory Controllers:

- **SD/SDIO Controller**
- **SDRAM Controller**
- **DDR / SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

Library Design Services

NanGate provides standard cell library design and optimization services both as a fully independent 3rd party IP vendor or as a partner in the development of high performance libraries.

The most common services provided are:

- Standard Cell Library Development
- Standard Cell Library and Design Optimization
- Performance Add-On Cells
- IP Migration: Generation of Library Variants
- Library Characterization Services

Standard Cell Library Development

NanGate has more than 20 years of experience in technology nodes from .35um down to 20nm and now working as partner with major foundries and fabless IC companies on 14nm. Our full featured standard cell libraries have demonstrated maximal density and routing performance. The cell schematic used on more complex cells also provides options for high performance or high density design optimizations. As part of the package, all industry standard views (CDL netlist, LEF, GDSII, Liberty, PEX Spice netlist, Verilog, VITAL, EDIF, OpenAccess db and others) are provided from a consistent database. Liberty files can be exported with all timing, power and noise models and for any operating condition (PVT corners). Here are examples of cells found in our standard cell libraries:

- Inverters, Buffers, Clock cells
- NAND, NOR, AND, OR cells
- AOI, OAI, AO, OA cells
- XNOR, XOR (buffered, unbuffered) cells
- MUX, IMUX cells
- D-type Latches (set, reset) and clock gate cells
- D-type Flops and Scan D-Type Flops (set, reset, both, enable)
- Half-Adder, Full-Adder cells

Special cells such as power management, retention and special operation cells can be added to the library. NanGate also counts with a vast repertory of cells for specific applications.

CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C/I3C Master/Slave**
- **SPI Master/Slave**
- **CAN/CAN FD bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**

Few advantages of using NanGate as a library IP provider and partner:

- High-quality DRC-clean and DFM-friendly layouts in very short time and lower costs – due to the use of our unique Library Creator Platform, the most advanced layout development tool suite;
- Quick library updates (including layout DRC clean-up) when design rules are still changing – technology exploration and PDK development phases;
- Flexibility in the specification of cells (functions, schematics);
- Option to create library variants (refer to IP migration below);
- Vast experience and know-how on standard cell libraries ranging from .35um to 14nm and in the area of application specific performance cells for CPUs and GPUs;
- Broad range of post-sales services such as library re-characterization – and very affordable.

Standard Cell Library and Design Optimization

NanGate has large experience working in processor core optimizations (mainly CPU and GPUs) collaborating with design teams in leading Tier-1 companies. Even foundries have used NanGate's design and library optimization flow to achieve higher performance in their benchmarks. In this area of IP optimization, NanGate provides mainly two independent yet complimentary services:

- Standard Cell Library Optimization
- Design Optimization

Getting the best performance library involves knowing the target application (design). And getting the best performance design relies on the quality of the standard cell library, macros and memories used. Even though each optimization can be done independently – and they do provide good results -, optimizing both libraries and design concurrently provides ultimate gains similar to or better than those seen in custom design flows.

KAL is representing Silvaco & Nangate in Israel.

www.KALtech.co.il

We are looking forward to hear from you.

Contact us for more information.

Tel 054-6305787/077-7199944 (Adi)

- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Modulation:

- **ADPSM**

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

Contact us for data sheet

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Until the next eNews,

Thanks you for your attention.

KAL