eNewsletter

**KAL - Large IP Cores:**

**VIP cores:**

- PCIe, USB, AMBA
- SD/SDIO, eMMC
- UniPro, I3C, Soundwire
- DDR 2/3/4, LPDDR, ONFI, SATA
- HDMI
- CAN, CANFD, FLexRay
- SPI, I2C, SMbus

**Military/Aerospace**

- 1553

**Multimedia**

- H.264
- JPEG

**Automotive:**

- CAN/CAN-FD
- FlexCAN
- FlexRay
- Lin

**AHB/APB Peripherals:**

- AHB/AXI/APB bridges
- Inter Connect complete IP

**Memory Controllers:**

- SD/SDIO Controller
- SDRAM Controller
- DDR / SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

**CPU Cores:**

- 32 bit - NEW

# Jivaro – Parasites Reduction and more

Jivaro is a solution dedicated to the reduction of parasitic networks. It helps backend physical verification teams (SPICE or FastSpice users) speeding up post layout simulation of huge parasitic extracted circuits, while keeping a very high accuracy.

Jivaro applies an ingenious mathematical approach to perform Model Order Reduction (MOR). Contrary to any heuristic technology, Jivaro allows to trade-off between accuracy and reduction with the user controlling the benefits. Jivaro can be applied with different thresholds on different parts of the design to maximize reduction. It can also offer more than MOR through the reduction of the number of active devices.

Jivaro has been proven to dramatically accelerate IC simulation while preserving an outstanding accuracy and has been adopted at leading IDM companies and fabless worldwide for technology nodes at 130nm and below. Jivaro was added to TSMC's Custom Reference Flow flow starting with 28nm. Jivaro is known to be used for designs at technology nodes of 10nm.

## Features:

• All types of parasitic netlist components: R, RC, RCC, RLC, RLCK, controlled sources
• Supports the following I/O formats: DSPF, SPEF, SPICE3, HSPICE, SPECTRE, CalibreView, reads and writes OpenAccess databases
• Supports temperature-dependent parasitic networks
• Can be applied differently on selected nets or sub-circuits within the hierarchy. Selection of the different nets can be along a path
• Compatible with all major EDA tools
• Additional capabilities for path-based reduction
• Multi-finger reduction
• Supports negative resistors

## Options:

- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

**Clock Synchronization:**

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

**Peripherals:**

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C/I3C Master/Slave**
- **SPI Master/Slave**
- **CAN/CAN FD bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

**PCI Bus Controllers and Peripherals:**

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

• Multi-threading
• Support of inductance and mutual inductance
• Seamless integration within the Cadence Virtuoso® platform (several possibilities)
• Graphical User Interfaces to pilot the reduction options
• Inline binaries for batch runs

## KAL is representing Silvaco in Israel.

www.KALtech.co.il

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We are looking forward to hear from you.
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Until the next eNews,

Thanks you for your attention.

KAL

**Modulation:**

- **ADPSM**

**Analog IP Cores:**

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

**Contact us for data sheet**

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