eNewsletter

KAL - Large IP Cores:

VIP cores:

- PCIe, USB, AMBA
- SD/SDIO, eMMC
- UniPro, I3C, Soundwire
- DDR 2/3/4, LPDDR, ONFI, SATA
- HDMI
- CAN, CANFDm FLexRay
- SPI, I2C, SMbus

Memory Controllers:

- **SD/SDIO Controller**
- **SDRAM Controller**
- **DDR / SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**

If Gate Level Simulation is interesting for you, you must be aware of this product:

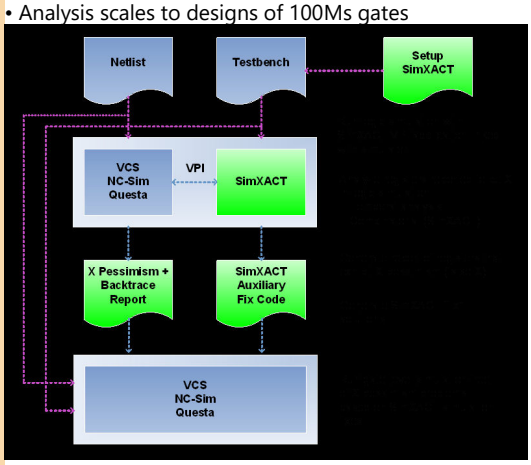
SimXACT

Gate Level Simulation

Accurate X Verification

SimXACT provide comprehensive solutions to effectively address the inherent limitations of handling non-determinism associated with X values in logic simulation which may render simulation results that do not match actual hardware operation. These X design bugs result in extra debug and analysis time or worse, if not caught prior to tape-out, non-functioning chips. Avery X verification uses unique hybrid formal methods to accurately analyze X propagations using real simulation.

• Run gate-level simulations free of X pessimism
• Automatically generate force/deposits for data and gated clocks
• Custom Verdi app to view X-pessimism fixes
• Diagnose occurrences of X optimism in RTL simulations warning of potential non-deterministic sequential behaviors
• Perform RTL and gate-level sequential X propagation tracing to enhance debug
• Accurately analyze and report X states during hardware reset and power transition sequences
• Static connection analysis detects connection errors at data, clock, or asynchronous reset/set
• Utilize plug'n'play setup
• Analysis scales to designs of 100Ms gates



X VERIFICATION IN GATE-LEVEL SIMULATION

During gate-level simulation it is common to find the simulation does not match the RTL simulation for several reasons:

- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Modulation:

- **ADPSM**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please**

• X-pessimism in the gate-level simulation creating false X situations
• X-optimism problems that went unnoticed in the RTL
• Clocking issues associated with clock divider and gated clock bring-up

SimXACT delivers an enhanced methodology for bringing up gate-level simulation more quickly and easily. SimXACT's patented technology can effectively analyze a simulation using a combinatorial analysis to determine if X values at D-inputs of DFF's or ICG's are real or false due to X-pessimism. SimXACT automatically eliminates the false Xs by generating a set of HDL forces/releases which allows the gate-level simulation to produce the correct results free of X-pessimism. The forces are applied on the fly during simulation to yield a one-pass solution. Uninitialized gated clock enables are another form of X-pessimism which can cause the gated clocks to be corrupted. SimXACT performs analysis of the gated clock fanout and generates the minimal deposit list on clock gater latches and downstream registers that will eliminate X-pessimism induced by X on gated clocks.

Other product that may be interesting for you:

Verification IPs

By Avery design Systems Inc

Avery provide Verification IP as native system Verilog to be used in all verification EDA tools for the major protocols and IP vendors:

High Speed IO	PCIe SR-IOV CCIX	USB xHCI SSIC/HSIC Dev/Hub PD 2.0	AMBA AXI3 AHB APB	 AXI4 ACE CHI
SSD/HDD	NVMe NVMf	UAS/BOT	SAS	SATA AHCI
Embedded Storage	UFS Device UFSHCI	eMMC eMMC HC	SD/SDIO SD HCI	UHS-II
Mobile	UniPro M-PHY	I3C Soundwire	CSI-2 DSI-2	C-PHY D-PHY
Memory	DDR5/4/3/2 LPDDR4/3/2 DFI-PHY	RDIMM/RCD LRDIMM/DB NVDIMM-P	HBM HMC	ONFI Toggle
Multimedia	HDMI	DP/eDP	DSC	DPI
Automotive	CAN/CAN FD	LIN	FlexRay	
Control Bus	I2C	SMBus	SPI	I2S

KAL is representing Avery in Israel.

www.KALtech.co.il

We are looking forward to hear from you.
Contact us for more information.

contact us.

- **We are expert in custom analog IP**

Contact us for data sheet

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Until the next eNews,

Thanks you for your attention.

KAL