eNewsletter

KAL - Large IP Cores:

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**

IP Review – USB2 w/ ULPI interface for ASIC/FPGA

The DUSB2-ULPI by Digital Core Design (dcd.pl) is a hardware implementation of a full/high-speed peripheral controller that in-terfaces to an ULPI bus transceiver. The DUSB2- ULPI contains a USB PID and address recognition logic, state machines to handle USB packets and transactions, endpoints number recognition logic and endpoints FIFO control logic. The DUSB2-ULPI is designed to support 12 Mb/s "Full Speed" (FS) and 480 Mb/s "High Speed" (HS) serial data trans-mission rates. The design is technology independ-ent and thus can be implemented in a variety of process technologies. This core strictly conforms to the USB Specification v 2.0 and ULPI v2.0. It is de-livered with **fully automated test bench** and **com-plete set of tests**, allowing easy package validation at each stage of SoC design flow.

MAINFEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Software configurable EP0 control endpoint size 8-64 bytes
- Software configurable 15 IN/OUT endpoints
  - *double buffering*
  - *configurable number of endpoints*
  - *configurable type of each endpoint: INTERRUPT, BULK or ISOCHRONOUS*
  - *configurable direction of each endpoint*
  - *configurable size of each endpoint: 8-1024 bytes*
- Supports ULPI Transceiver Macrocell Interface
- Synchronous RAM interface for FIFOs
- Suspend and resume power management functions
- Simple interface allows easy connection to 8, 16, 32- bit CPU
- Allows operation from a wide range of CPU clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Scan test ready

- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Modulation:

- **ADPSM**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

Contact us for data sheet

APPLICATIONS

Human Interface Devices like keyboards, mousses or game peripherals
- Mass Storage devices like flash disks, mp3 or mp4 players
- GPS navigation systems
- Digital Cameras
- Cellular phones
- Audio devices like microphones and speakers
- Printers
- Scanners

More information:

http://dcd.pl/ipcore/1250/dusb2-ulpi/

KAL is representing DCD.

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Until the next eNews,

Thanks you for your attention.

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