eNewsletter

KAL - Large IP Cores:

VIP cores:

- **PCIe, USB, AMBA**
- **SD/SDIO, eMMC**
- **UniPro, I3C, Soundwire**
- **DDR 2/3/4, LPDDR, ONFI, SATA**
- **HDMI**
- **CAN, CANFDm FLexRay**
- **SPI, I2C, SMbus**

Military/Aerospace

- **1553**

Multimedia

- **H.264**
- **JPEG**

Memory Controllers:

- **SD/SDIO Controller**
- **SDRAM Controller**
- **DDR / SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**

Clock Synchronization:

BMC IP is available for customers who want to implement the 1553 interface inside their system.

The IP can be linked to any FPGA device. It can be configured with **single or multiple channels and protocols**.

BMC advanced MIL-STD-1553 IP core come with a set of enhanced capabilities allowing for your communication bus to have real time digital wiring fault detection and prognosis, so your aircraft will experience minimum downtime.

The cores are suitable for any **MIL-STD-1553** application, including direct replacement of existing ICs. It includes multiple receive/transmit buffers for 1553 applications, sub-address filtering, error bit detection and/or injection, programmable conditions for RT status error bit, Long LOOP Test error and many others.

There are a variety of ARINC protocols but the most common is **ARINC 429**/575/572/582/615.., a 32 bit data protocol. It has a two wire line with true and complement data. The electrical signals use a NRZI format. Some equipment requires a parity bit in the bit stream (odd or even), others do not. BMC-IP has implemented all these conditions.

There also a number of ARINC protocols with 6 wires; 3 signals twisted pair, like **ARINC 561, ARINC 571** and **ARINC 581**. The electrical signals use a NRZ format. BMC-IP supports these protocols as well.

The ARINCs receive/transmit IP interface is based on a 32 cache FIFO each with 32 bit words to protecxt the system from data overlap.

ARINC 453/708 software operates exactly as **ARINC**

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588Master/Salve
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

Peripherals:

- HDLC/SDLC
- Smart Card Reader Unit
- EEPROM SPI Ctrl
- LCD Ctrl
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN/CAN FD bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Salve
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Modulation:

- ADPSM

AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller

2-6 wires protocols.

ARINC 573/717 has programmable transmit/receive rate; 64/128/256/512 words (10 bits) p/second and error injection as well. It channel is independently configurable through software and operates according to Harvard biphase protocol.

The BMC ARINC-IP offers **UNLIMITED independent transmitters and independent receivers in the same core**.

BMC can customize the IP according to customer requirements.

KAL is representing BMC Communications Corp. in Israel.

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We are looking forward to hear from you.
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Until the next eNews,

Thanks you for your attention.

KAL

- **AXI Bus Master/Slave**

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

Contact us for data sheet