Contact Us

eNewsletter

We are pleased to provide you with the latest news from our partners. We have a lot of customers like

Until then, we thank you for your continued support!

**Large IP Cores:**

**CPU Cores:**

- 8 bit - 8051
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- DSP – MSP430
- 32 bit - ARM 9xx/11xx

**Memory Controllers:**

- SD/SDIO 2.0/3.0 Controller
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

**Clock Synchronization:**

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Salve
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

# The syn1588® board product family by Oregano Systems will release in Q1/2010 a new version of NICs driver and stack.

## Features

Improved system throughput (up to 100%)
Second PCI BAR for efficient access to syn1588® registers on application level
Event FIFO with 16 entries for EVENT Time Stamp 0 allowing to capture external event bursts
Trigger FIFO with 16 entries for TRIGGER0 allowing to generate arbitrary high frequency
pulse trains.
Simplfiet system configuration
syn1588® PTP Stack optionally synchronizes system clock
FreeBSD support added
Multiple instances of syn1588 PTP stack running in parallel
Full support for IEEE1588 telcom profile

### Improved System Throughput

The system throughput has been optimized by several measures in both hardware and software to gain an overall improvement of about

**Peripherals:**

- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

**PCI Bus Controllers and Peripherals:**

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

**Memory Library:**

- **CAM**
- **Low Power SRAM Solutions**
- **Low Power Register Files**
- **Low Power ROM**
- **Custom per customer need**

**Encryption:**

12% on the average.

**Second PCI BAR**

The syn1588®Clock_M registers are made available in parallel via a second BAR on the PCI interface. This allows using another software driver offering a faster access to the registers. About 90% of the total register access time accounts to the operating system. Using this feature this time can but cut down. This feature is important for all customers that timestamp software events by reading the TIME registers.

**Event FIFO**

The EVENT0 input (EVENTTIME0 registers) will be improved by adding a 16 entry FIFO. Now dense external events can be properly timestamped without real-time requirements for the software.

**Trigger FIFO**

The TRIGGER0 output (TRIGTIME0 registers) will be improved by adding a 16 entry FIFO. Now dense events can be precisely scheduled without real-time requirements for the software.

**Free BSD Suppport**

Starting with this release we also add support for Free BSD.

**Easier System Configuration**

The syn1588® PCI/PCIe NIC driver now automatically configures the syn1588® PCI/PCIe NIC with its syn1588® clock frequency.

**PTP Stack Synchronizes System Clock**

The syn1588® PTP Stack now optionally synchronizes the system clock to the accurate synchronized hardware clock after performing some basic plausibility checks.

**Free BSD Suppport**

Starting with this release we also add support for Free BSD.

**Multiple Instances of syn1588® PTP Stack**

In the past multiple syn1588® PCI/PCIe NICs could have been added to a single PC but only one instance of the syn1588® PTP Stack could be executed on this PC. Now multplite instance oi the syn1588® PTP stack may be executed on a single node.

**IEEE1588 Telecom Profile**

Starting with this release we fully support the IEE1588 telecommunications profile.

**Contact us for more information or replay for this email.**

- AES 128bit/256bit
- ECC

**AHB/APB Peripherals:**

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

**MIPS CPU Interface:**

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

**PowerPC CPU Interface:**

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

**ARC CPU Interface:**

- ARC - Peripheral Controller for ARCtangent
- ARC – ARCtangent to PCI host Bridge

**Analog IP Cores:**

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

**Contact us for data sheet**

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